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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6311204 B1

L24: Entry 1 of 9

File: USPT

Oct 30, 2001

US-PAT-NO: 6311204

DOCUMENT-IDENTIFIER: US 6311204 B1

TITLE: Processing system with register-based process sharing

DATE-ISSUED: October 30, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Christopher	Santa Clara	CA		

US-CL-CURRENT: 709/100; 345/502, 345/558

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 2. Document ID: US 6088355 A

L24: Entry 2 of 9

File: USPT

Jul 11, 2000

US-PAT-NO: 6088355

DOCUMENT-IDENTIFIER: US 6088355 A

TITLE: Processing system with pointer-based ATM segmentation and reassembly

DATE-ISSUED: July 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Christopher	Santa Clara	CA		
Adams; Christopher	Palo Alto	CA		

US-CL-CURRENT: 370/392; 370/397

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 3. Document ID: US 5953691 A

L24: Entry 3 of 9

File: USPT

Sep 14, 1999

US-PAT-NO: 5953691

DOCUMENT-IDENTIFIER: US 5953691 A

TITLE: Processing system with graphics data prescaling

DATE-ISSUED: September 14, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Christopher	Santa Clara	CA		

US-CL-CURRENT: 702/198; 348/391.1, 348/396.1, 709/214

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMJC
Draw Desc	Image									

☐ 4. Document ID: US 5926647 A

L24: Entry 4 of 9

File: USPT

Jul 20, 1999

US-PAT-NO: 5926647

DOCUMENT-IDENTIFIER: US 5926647 A

TITLE: Processing system with dynamic alteration of a color look-up table

DATE-ISSUED: July 20, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Adams; Christopher	Palo Alto	CA		
Charles; Gordon A.	Palo Alto	CA		
Mills; Christopher	Santa Clara	CA		

US-CL-CURRENT: 712/36; 345/589, 345/600, 345/601, 710/26

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMJC
Draw Desc	Image									

☐ 5. Document ID: US 5923385 A

L24: Entry 5 of 9

File: USPT

Jul 13, 1999

US-PAT-NO: 5923385

DOCUMENT-IDENTIFIER: US 5923385 A

TITLE: Processing system with single-buffered display capture

DATE-ISSUED: July 13, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Christopher	Santa Clara	CA		
Ayers; Thomas R.	San Jose	CA		

US-CL-CURRENT: 348/715; 348/439.1, 348/718

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 6. Document ID: US 5889949 A

L24: Entry 6 of 9

File: USPT

Mar 30, 1999

US-PAT-NO: 5889949

DOCUMENT-IDENTIFIER: US 5889949 A

TITLE: Processing system with memory arbitrating between memory access requests in a set top box

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Charles; Gordon A.	Palo Alto	CA		

US-CL-CURRENT: 709/214; 712/42

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 7. Document ID: US 5793427 A

L24: Entry 7 of 9

File: USPT

Aug 11, 1998

US-PAT-NO: 5793427

DOCUMENT-IDENTIFIER: US 5793427 A

TITLE: Processing system with delta-based video data encoding

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Christopher	Santa Clara	CA		
Ayers; Thomas R.	San Jose	CA		
Lenihan; Michael P.	Sunnyvale	CA		

US-CL-CURRENT: 348/391.1; 348/396.1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 8. Document ID: US 5790842 A

L24: Entry 8 of 9

File: USPT

Aug 4, 1998

US-PAT-NO: 5790842

DOCUMENT-IDENTIFIER: US 5790842 A

TITLE: Processing system with simultaneous utilization of multiple clock signals

DATE-ISSUED: August 4, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Charles; Gordon A.	Palo Alto	CA		
Mills; Christopher	Santa Clara	CA		

US-CL-CURRENT: 713/600

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 9. Document ID: US 5530874 A

L24: Entry 9 of 9

File: USPT

Jun 25, 1996

US-PAT-NO: 5530874

DOCUMENT-IDENTIFIER: US 5530874 A

TITLE: Network adapter with an indication signal mask and an interrupt signal mask

DATE-ISSUED: June 25, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Emery; Scott A.	San Jose	CA		
Petersen; Brian	Los Altos	CA		
Sherer; W. Paul	Sunnyvale	CA		

US-CL-CURRENT: 710/262; 710/267, 710/49

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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Term	Documents
MASK\$	0
MASK.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	313211
MASKA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	235
MASKABEL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
MASKABILITY.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	11
MASKABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2391
MASKABLEINTERRUPT.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
MASKABLE/NON.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
MASKABLE/NONMASKABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
MASKABLE/NON-MASKABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
MASKABLE/UNMASKABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
(L23 AND (MASK\$ NEAR5 DATA)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	9

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Search Results - Record(s) 1 through 8 of 8 returned.☐ 1. Document ID: US 6154384 A

L7: Entry 1 of 8

File: DWPI

Nov 28, 2000

DERWENT-ACC-NO: 2001-217365

DERWENT-WEEK: 200122

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TITLE: Ternary content addressable memory for network routers,
pattern recognition, has comparator provided with transistors to
compare data stored in main memory cell with mask data, for masking
data stored in main cell

INVENTOR: KHANNA, S; NATARAJ, B S ; SRINIVASAN, V

PRIORITY-DATA: 1999US-0439317 (November 12, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6154384 A	November 28, 2000		007	G11C015/00

INT-CL (IPC): G11 C 15/00

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Clip Img	Image									

☐ 2. Document ID: JP 2000259139 A

L7: Entry 2 of 8

File: DWPI

Sep 22, 2000

DERWENT-ACC-NO: 2000-633226

DERWENT-WEEK: 200061

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TITLE: Image display device for network applications, converts
transmitted data into many images according to mask pattern of
specified format

PRIORITY-DATA: 1999JP-0057575 (March 4, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000259139 A	September 22, 2000		007	G09G005/00

INT-CL (IPC): G09 G 3/20; G09 G 5/00; H04 N 1/38; H04 N 7/16

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Clip Img	Image							

KVMC

☐ 3. Document ID: JP 2000011023 A

L7: Entry 3 of 8

File: DWPI

Jan 14, 2000

DERWENT-ACC-NO: 2000-151650

DERWENT-WEEK: 200014

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TITLE: Mask layout pattern data verification method - has search unit which searches path from predetermined network to ground potential, extracts parasitic element on path and outputs network list to list file

PRIORITY-DATA: 1998JP-0174704 (June 22, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000011023 A	January 14, 2000		011	G06F017/50

INT-CL (IPC): G03 E 1/08; G06 E 17/50

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Clip Img	Image							

KVMC

☐ 4. Document ID: JP 09282350 A

L7: Entry 4 of 8

File: DWPI

Oct 31, 1997

DERWENT-ACC-NO: 1998-024063

DERWENT-WEEK: 199803

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TITLE: Mask ROM data generator used in layout pattern manufacture, logic simulation model, ASIC - obtains whole area network of mask ROM corresponding to each block division data by referring partial network in hierarchical manner

PRIORITY-DATA: 1996JP-0095259 (April 17, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 09282350 A	October 31, 1997		007	G06F017/50

INT-CL (IPC): G06 E 17/50

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Clip Img	Image							

KVMC

☐ 5. Document ID: JP 09044559 A

L7: Entry 5 of 8

File: DWPI

Feb 14, 1997

DERWENT-ACC-NO: 1997-184499

DERWENT-WEEK: 199717

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TITLE: Layout verification method for large scale integration mask pattern production - by comparing internal and external simulation program with integrated circuit emphasis network list derived from layout pattern, correspondence relationship of circuit diagram data is verified

PRIORITY-DATA: 1995JP-0211227 (July 27, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 09044559 A	February 14, 1997		004	G06F017/50

INT-CL (IPC): G06 E 17/50

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Clip Img	Image								

☐ 6. Document ID: JP 08221457 A

L7: Entry 6 of 8

File: DWPI

Aug 30, 1996

DERWENT-ACC-NO: 1996-447533

DERWENT-WEEK: 199645

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TITLE: Layout pattern generator for writing ROM code to integrated circuit e.g. large scale integration built in mask ROM - has logic simulation execution unit that performs logic simulation of whole chip on integrated circuit corresp. to read test-pattern data and extracted network list data

PRIORITY-DATA: 1995JP-0021580 (February 9, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 08221457 A	August 30, 1996		006	G06F017/50

INT-CL (IPC): G06 E 17/50; H01 L 21/8246; H01 L 27/112

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Clip Img	Image								

☐ 7. Document ID: JP 06110971 A

L7: Entry 7 of 8

File: DWPI

Apr 22, 1994

DERWENT-ACC-NO: 1994-170766

DERWENT-WEEK: 199421

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TITLE: Data extraction device for extracting parasitic element in design of large scale integrated circuit - reads mask-pattern data and information about parasitic element and uses network list for simulation based on data requested for processing input NoAbstract

PRIORITY-DATA: 1992JP-0283494 (September 30, 1992)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 06110971 A	April 22, 1994		006	G06F015/60

INT-CL (IPC): G06F 15/20; G06F 15/60; H01L 21/82

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Clip Img	Image								

☐ 8. Document ID: JP 05031958 A

L7: Entry 8 of 8

File: DWPI

Feb 9, 1993

DERWENT-ACC-NO: 1993-088382

DERWENT-WEEK: 199311

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TITLE: Picture forming device improving picture quality - eliminates need to have mask pattern by using neural network which can correct picture data for pattern other than learnt pattern
NoAbstract

PRIORITY-DATA: 1991JP-0193263 (August 1, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 05031958 A	February 9, 1993		015	B41J002/485

INT-CL (IPC): B41J 2/485; G06F 15/18; G06F 15/72; G06G 7/60; H04N 1/40

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Clip Img	Image								

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Term	Documents
PATTERNS1	0
PATTERN.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	162617
PATTERNA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
PATTERNE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	3
PATTERNI.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
PATTERNM.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
PATTERNS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	29416
PATTERN/ DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
PATTERN: DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	32
MASK.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	61589
((PATTERNS1 AND MASK AND DATAS AND NETWORKS). TI.) USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	8

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Search Results - Record(s) 1 through 1 of 1 returned.

☒ 1. Document ID: US 6111658 A

9: Entry 1 of 1

File: USPT

Aug 29, 2000

US-PAT-NO: 6111658

DOCUMENT-IDENTIFIER: US 6111658 A

TITLE: Dither method and printing apparatus

DATE-ISSUED: August 29, 2000

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Tabata; Yuji

Higashiyamato

JPX

US-CL-CURRENT: 358/19; 358/457, 358/460, 358/535

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KMIC

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Term	Documents
(8 AND 1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	1
(L8 AND L1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	1

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Term	Documents
MASK\$	0
MASK DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	313211
MASKA DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	235
MASKABEL DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
MASKABILITY DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	11
MASKABLE DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2391
MASKABLEINTERRUPT DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
MASKABLE/NON DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
MASKABLE/NONMASKABLE DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
MASKABLE/NON-MASKABLE DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
MASKABLE/UNMASKABLE DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
.....	
MASK\$(MASK-FITTING).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	pickup term
(L23 AND (MASK\$ NEAR5 DATA)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	9

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L24

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Search History

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<i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>			
<u>L24</u>	L23 and (mask\$ near5 data)	9	<u>L24</u>
<u>L23</u>	L22 and stor\$	18	<u>L23</u>
<u>L22</u>	L18 and pattern\$1	18	<u>L22</u>
<u>L21</u>	L18 and (pattern\$1 same algorithm\$)	0	<u>L21</u>
<u>L20</u>	L18 and (stor\$ same pattern\$1)	0	<u>L20</u>
<u>L19</u>	L18 and (stor\$ near5 pattern\$1)	0	<u>L19</u>
<u>L18</u>	L17 and 'state machine'	29	<u>L18</u>
<u>L17</u>	l15 and 'data frame'	92	<u>L17</u>
<u>L16</u>	L15 and 'pattern match logic circuit'	0	<u>L16</u>
<u>L15</u>	L14 and (network\$ near5 interfac\$)	868	<u>L15</u>
<u>L14</u>	'first memory' and 'second memory'	25490	<u>L14</u>
<u>L13</u>	L12 and (mark\$ near5 pattern\$1)	0	<u>L13</u>
<u>L12</u>	(memory and network\$ and pattern\$1).ti.	73	<u>L12</u>
<u>L11</u>	('pattern matching' same 'network').ti.	29	<u>L11</u>
<u>L10</u>	('pattern matching' same 'network').ti,ab.	101	<u>L10</u>
<u>L9</u>	L8 and l1	1	<u>L9</u>
<u>L8</u>	(mask\$ near5 RAM) same (pattern\$1 near5 RAM)	46	<u>L8</u>
<u>L7</u>	(pattern\$1 and mask and data\$ and network\$).ti.	8	<u>L7</u>
<u>L6</u>	L5 and l1	0	<u>L6</u>
<u>L5</u>	(multi\$ near5 memories) same (pattern\$1 near5 mask\$1)	13	<u>L5</u>
<u>L4</u>	L3 and ((pattern\$1) same (mask data))	1	<u>L4</u>
<u>L3</u>	(network\$ and interfac\$).ti.	5633	<u>L3</u>
<u>L2</u>	l1 and ((second memory) near5 (mask data\$))	1	<u>L2</u>
<u>L1</u>	(first memory) near5 (pattern\$1)	807	<u>L1</u>

END OF SEARCH HISTORY